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<input type="checkbox"/>	L16	L15 and (HSG or hemispherical)	9
<input type="checkbox"/>	L15	L14 and capacitor	55
<input type="checkbox"/>	L14	(tungsten adj nitride) same (aluminum adj oxide)	211
<input type="checkbox"/>	L13	L12 and nitride and (aluminum or AlO3)	204
<input type="checkbox"/>	L12	(L11 or L9 or L8 or L7)	1175
<input type="checkbox"/>	L11	L10 not L9	197
<input type="checkbox"/>	L10	L8 and (HSG or hemispherical).clm.	370
<input type="checkbox"/>	L9	L8 and (HSG or hemisperical).clm.	173
<input type="checkbox"/>	L8	438/398.ccls.	801
<input type="checkbox"/>	L7	(L5 or L6) and (HSG or (hemispherical adj grain\$2))	898
<input type="checkbox"/>	L6	257/532,534.ccls.	2129
<input type="checkbox"/>	L5	438/396-399.ccls.	5318
<input type="checkbox"/>	L4	((HSG with (etch\$5 or HF)) same (native adj oxide)) and (aluminum adj oxide) and nitride	6
<input type="checkbox"/>	L3	L2 and HF	44
<input type="checkbox"/>	L2	(open\$3 with grains) and HSG	133
<input type="checkbox"/>	L1	(HF with grains) and capacitor and HSG	22

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IEE CNF	IEE Conference Proceeding				
IEEE STD	IEEE Standard				

Article Information

1. **Fabrication and performance of selective HSG storage cells for 256 Mb and 1 Gb DRAM applications**
 Banerjee, A.; Wise, R.L.; Plumton, D.L.; Bevan, M.; Pas, M.F.; Crenshaw, D.L.; Aoyama, S.; Mansuripur, M.
Electron Devices, IEEE Transactions on
 Volume 47, Issue 3, March 2000 Page(s):584 - 592
 Digital Object Identifier 10.1109/16.824734
[AbstractPlus](#) | [References](#) | Full Text: [PDF\(1088 KB\)](#) IEEE JNL

2. **Micro villus patterning (MVP) technology for 256 Mb DRAM stack cell**
 Ahn, J.H.; Park, Y.W.; Shin, J.H.; Kim, S.T.; Shim, S.P.; Nam, S.W.; Park, W.M.; Shin, H.B.; Choi, C.; Kwon, O.H.; Hwang, C.G.;
VLSI Technology, 1992. Digest of Technical Papers. 1992 Symposium on
 2-4 June 1992 Page(s):12 - 13
 Digital Object Identifier 10.1109/VLSIT.1992.200619
[AbstractPlus](#) | Full Text: [PDF\(192 KB\)](#) IEEE CNF

3. **An advanced technique for fabricating hemispherical-grained (HSG) silicon storage electrodes**
 Watanabe, H.; Tatsumi, T.; Ikarashi, T.; Sakai, A.; Aoto, N.; Kikkawa, T.;
Electron Devices, IEEE Transactions on
 Volume 42, Issue 2, Feb. 1995 Page(s):295 - 300
 Digital Object Identifier 10.1109/16.370066
[AbstractPlus](#) | Full Text: [PDF\(740 KB\)](#) IEEE JNL

4. **Capacitance enhancement techniques for sub-100 nm trench DRAMs**
 Gutsche, M.; Seidl, H.; Luetzen, J.; Birner, A.; Hecht, T.; Jakschik, S.; Kerber, M.; Leonhardt, M.; M.; Reisinger, H.; Rongen, S.; Saenger, A.; Schroeder, U.; Sell, B.; Wahl, A.; Schumann, D.;
Electron Devices Meeting, 2001. IEDM Technical Digest. International
 2-5 Dec. 2001 Page(s):18.6.1 - 18.6.4
 Digital Object Identifier 10.1109/IEDM.2001.979524
[AbstractPlus](#) | Full Text: [PDF\(294 KB\)](#) IEEE CNF

5. **HSG storage capacitor dielectric reliability of 0.13 /spl mu/m embedded DRAM CMOS technology**
 Bruyere, S.; Roy, D.; Jacques, D.; Boccaccio, C.;
Reliability Physics Symposium Proceedings, 2003. 41st Annual. 2003 IEEE International
 30 March-4 April 2003 Page(s):298 - 302
 Digital Object Identifier 10.1109/RELPHY.2003.1197761
[AbstractPlus](#) | Full Text: [PDF\(398 KB\)](#) IEEE CNF

□ 6. A cost effective embedded DRAM integration for high density memory and high performance technology node and beyond
Daewon Ha; Dongwon Shin; Gwan-Hyeob Koh; Jaegu Lee; Sanghyeon Lee; Yong-Seok Ahn; Hong-Chung Chung; Kinam Kim;
Electron Devices, IEEE Transactions on
Volume 47, Issue 7, July 2000 Page(s):1499 - 1506
Digital Object Identifier 10.1109/16.848299

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